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CYGNUS-ZN1 System-on-Module



Description

Artron Cygnus-ZN1 SoM is based on the Xilinx Zynq XA7Z020-1CLG400Q SoC. The Xilinx Zynq family features a dual-core ARM Cortex processor-based processing system (PS) and programmable logic (PL) in a single integrated device. Cygnus-ZN1 SoM is populated entirely with industrial grade electronic components and is suitable for use in applications demanding harsh environmental requirements.

The particular model used here has PL size equivalent to 53.200 LUTs and includes 130 PS and 125 PL IO pins. 111 of the PL IOs are connected to the IO connectors, of which 25 pins are from Bank-13, 46 pins are from Bank-34 and 40 pins are from Bank-35.

The 26 PS MIO pins are connected to the IO connectors for the RGMII Ethernet interface, 4 PS MIO pins for PJTAG interface and 2 PS MIO pins for the UART interface.

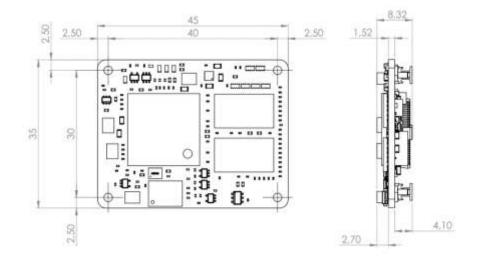
Features

- Xilinx Zyng® XA7Z7020 Programmable SoC (CLG400 Package)
 - Dual-core ARM Cortex-A9 MPCore™ with CoreSight™
 - NEON™ & Single / Double Precision Floating Point for each processor
 - Xilinx Artix-7 FPGA with 53.200 LUTs, 106.400 Flip-Flops
 - AES and SHA 256b for Boot Code and Programmable Logic Configuration, Decryption, and Authentication
- 124 programmable PL I/O pins
- 4 PS MIO Pins
- 8Gbit 1066Mb/s DDR3 RAM
- 256Mbit QSPI Flash Memory
- 3 connectors, 2x100 pin, 1x50 pin, (Samtec ST5) high mating cycle capable –
- Wide Operating Temperature Range (-40°C to 85°C)
- Petalinux compiled BSP and reference designs available on our website.





Mechanical Properties



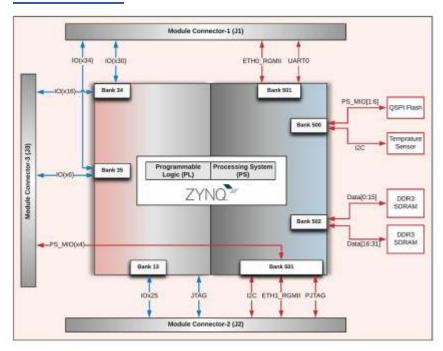
Parameter	Dimensions
Size	45x35 mm
Top Height	4.2 mm (incl.PCB)
Bottom Height	4.1 mm
Mounting Holes	Ø 2.5 mm
Weight	11.5 gr

Ordering Information

Part Number	Definition	Pricing
ART-CYG-ZN1Q-0720	SoM equipped with XA7Z020	
ART-CYG-ZN1Q-0714	SoM equipped with XA7Z014S	Contact us.
ART-CYG-ZN1Q-0710	SoM equipped with XA7Z010	
ART-CYG-ZN1Q-0707	SoM equipped with XA7Z007S	
ART-CYG-ZN2-CB*	Carrier Board	
ART-CYG-ZN2-HS*	Heatsink	

^{*} Artron Cygnus-ZN1 and Cygnus-ZN2 uses same carrier board and heatsinks.

Block Diagram



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